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A high efficiency and high speed charge of Li-Ion battery charger interface using switching-based technique in 180 nm CMOS technology

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Article Info

ABSTRACT

In this work, the design and analysis of new Li-Ion battery charger interface using the switching-based technique is proposed for high efficiency, high speed charge and low area. The high efficiency, the lower size area and the fast charge are the more important norms of the proposed Li-Ion battery charger interface. The battery charging is completed passes to each charging mode: The first mode is the trickle charge mode (TC), the second mode is the constant current mode (CC) and the last mode is the constant voltage mode (CV), in thirty three minutes. The new Li-Ion battery charger interface is designed, simulated and layouted in Cadence software using TSCM 180 nm CMOS technology. With an input voltage V_{IN} = 4.5 V, the output battery voltage (V_{BAT}) may range from 2.7 V to 4.2 V and the maximum charging battery current (I_{BAT}) is 1.7 A. The peak efficiency reaches 97% and the total area is only 0.03mm².

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1. INTRODUCTION

The Battery is a necessary element to supply the electricity-powered portable devices, for example, cellular phone, Laptop, tablets, etc. In addition, decreasing the power consumption to widen the operational life and time, the charging is another critical issue for the battery [1]. Slower charging is considered as wasting time. However, the degradation of battery life and the increase in temperature are caused by a fast charging [2]. The Li-Ion battery is mostly utilized in the automotive feild especialy in the production of electrical vehicles, respecting the global policy on the application of renewable energies and alternative energies [3]-[5].

Thus, the Ni-Cd and the Ni-MH batteries are substitute of the Li-Ion batteries, that due of their high performance [6], but to this day, the Li-Ion batteries are the more used and popular rechargeable batteries, and controls the mobile battery market [7]. Further more, to full-full the purpose of obtaining a reduce production cost, the high efficiency and the necessity of a low complexity of the Li-Ion battery charger interface (BCI) are highly important [8].

The Li-Ion battery renowned as the best energy storage that solve the need of a low cost, a light weight and a long operation time [1]. Therefore, the charging solution for the Li-Ion battery has appealed so intense research efforts regardless in the industry or in the academia [6], [9], [10]. The charger solutions well known are essentially classified into two types, Figure 1 shows the LDO (Low-Dropout) based charger and the switching-based charger [11].
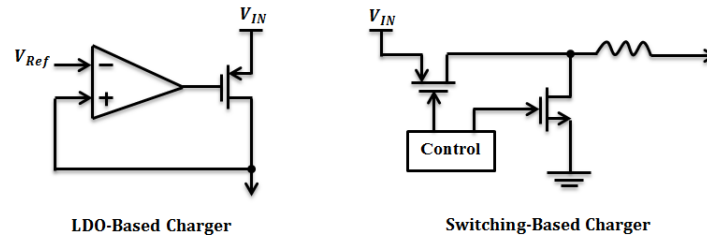

Figure 1. The LDO (low-dropout) based charger and the Switching-based charger [11]

The LDO-based charger achieves the benefit of simplicity at the trouble of a poor efficiency. The LDO-based charger respondent for such requests cause of its low current ripple and it may be inserted into the chip without a descriptive component [12]. The lower efficiency is a great problem for it, so the utilization of the Power-MOS as a variable current source is a solution of its low efficiency and also to minimize it dropout [13]. The switching based requires an advanced circuit design to realize a high efficiency, it gives a wide range of the input/output voltage [14]. Further more the switching based is costing a lot of drawbacks, like a worse noise repudiation as of the ripple at a switching rate, and rise power consumption [15].

In addition, these charging systems are typically integrated into a single chip to minimize circuit design complexity through the improvement of CMOS technology. Then, the battery charger is integrated into a System-on-Chip (SoC) to reduce the effect of ripple and noise [15]. Figure 2 shows the charging modes of Li-Ion battery that's consisted of four stages: the first one is the trickle charge (TC), the second one is the constant current (CC) charge, the third one is the constant voltage (CV) charge and the last one is the charge termination [16], [17].
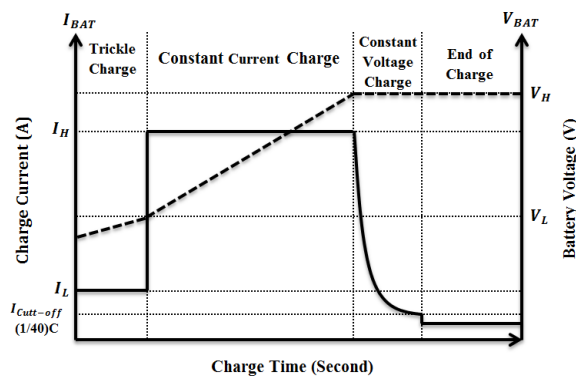

Figure 2. The charging modes of Li-Ion battery

The TC charge mode is activated when the battery voltage (V_{BAT}) is reduced than the low voltage (V_L), the battery current is kept at a constant low value (0.1C, C represents the capacity of the battery and its unit is (Ah) ampere-hours) to protect the battery from being damaged by an overheating. The CC charge mode is selected when V_{BAT} is between the low voltage (V_L) and the high voltage (V_H), it minimizes the charging time because the battery is charged with a high CC (0.1C-1C).

The CV charge mode is activated when V_{BAT} rise up to the specs value of the V_H, which make the charging current (I_{BAT}) falls to the cut-off (0.02C-0.07C) and the charge process ends. We presented this article at the following: Section II proposes the charging circuit of Li-Ion battery charger interface; Section III presents the simulation results of our charging circuit; and we conclude in Section IV.

2. PROPOSED CHARGING CIRCUIT OF LI-ION BATTERY CHARGER INTERFACE

Until now, there are numerous research articles have offered a different architectures in order to generate a constant output supply voltage for the Li-Ion BCI using CMOS technology, but their power efficiency is comparatively low due to an increase power loss of the Power-MOSFET [17]-[21]. As a solution of this problem we are going to control the each mode via its identical control signal to improve the power efficiency that will contribute to adapting between the supply voltage of charging and the V_{BAT}. A proposed charging circuit of Li-Ion BCI is illustrated in Figure 3 which includes seven sub-circuits: the mode control, the currents reference, the charge control, the gate driver, the level shifter and the current sensing.
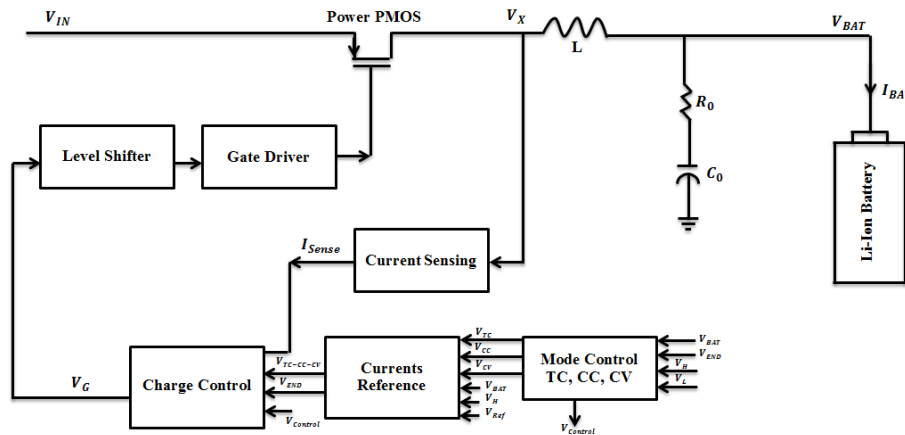

Figure 3. The proposed charging circuit of Li-Ion battery charger interface (BCI)

The mode control block is concepted to define the charging modes (TC, CC and CV) by comparing the V_{BAT} with the V_H and the V_L, which are generated from a band-gap block. In other hand the currents reference block produces a desired currents matching to the mode control output voltage. The latter block is followed by a charge control block utilized for comparing between the current sensor I_{sense} and the reference currents to generate the gate voltage (V_G) which assist to control the P-PMOS thanks to the level-shift with a gate-driver circuit. That maintains a constant voltage difference among the supply voltage (V_{IN}) and the V_{BAT}. The operating principle of each block has been described below.

2.1. Mode Control

The mode control circuit is shown in Figure 4. The mode control block circuit is a logic control system consist of two levels from output voltage: a high voltage that means logic level equal '1' and a low voltage that means logic level equal '0'. It contributes to define the V_{BAT} and to produce the control signals (V_{TC}, V_{CC}, V_{CV}) respectively. The trickle charge voltage (V_{TC}), the constant current voltage (V_{CC}) and the constant voltage voltage (V_{CV}) are resulting from a comparison (by two high speed comparator) of the V_{BAT} with the reference voltages (the V_H and the V_L). Therefore, when V_{BAT} is lower than the V_L, being only the V_{TC} active. When V_{BAT} is higher or equal than the V_L and lower than the V_H, being only the V_{CC} active. And when V_{BAT} is higher or equal than the V_H, being only the V_{CV} active.

Also, the control voltage signal ($V_{Control}$) is sent to the charge control block for generating a charge current in the corresponding charge mode. Figure 5 shows the waveforms of the control signals (V_{TC}, V_{CC}, V_{CV}), the I_{BAT} and the V_{BAT}. We can observed from Figure 5 that in the TC mode, only the V_{TC} is set to 'ON'. In the CC mode, only the V_{CC} is set to 'ON'. And in the CV mode, only the V_{CV} is set to 'ON'.
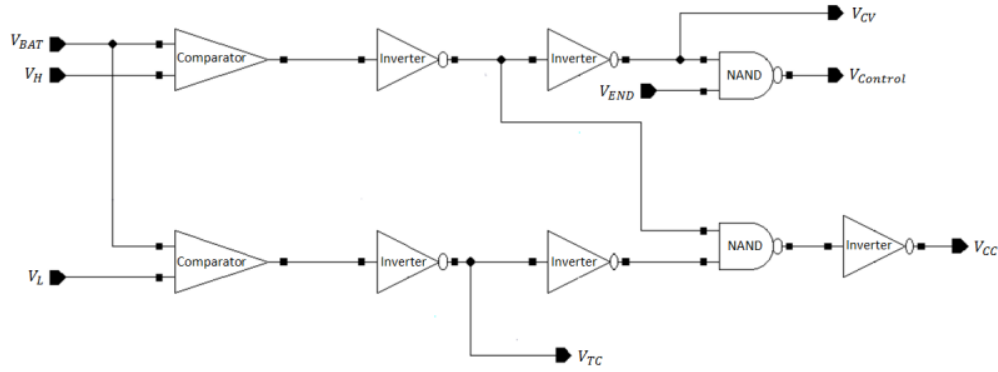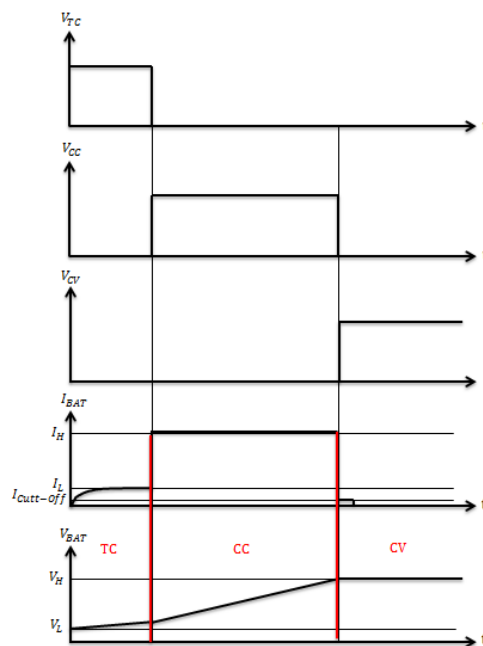
Figure 4. Schematic of the mode control block under CADENCE software

Figure 5. Waveforms of the control signals (V_{TC}, V_{CC}, V_{CV}), the battery current (I_{BAT}) and the battery voltage (V_{bat})

2.2. Currents Reference

Figure 6 shows the currents reference circuit under CADENCE software. It consists of an OpAmp and a Comparator to produce a current reference I_{Ref} which is determined in the equation:

$$I_{Ref} = \frac{V_{Ref}}{R_{Ref}} \tag{1}$$

The first current mirror system consisting of the PMOS transistors (PM2, PM3, PM4, PM5) used in the design, assist to produce a trickle charge current (I_{TC}), a constant current current (I_{CC}) and a cut-off current ($I_{Cutt-off}$), that are proportional to I_{Ref}. Also, they are utilized as a references proportional in the TC mode, the CC mode and the end of the charge mode, respectively. As well, when the V_{BAT} reaches 4.25V, the high speed comparator with the second current mirror system consisting of a PMOS transistors (PM0, PM1) used in the design, starts to produce a constant voltage current (I_{CV}) which is decreasing from the I_{CC} to the $I_{Cut-off}$. The I_{CV} is utilized as a reference proportional in the CV mode. The V_{TC}, the V_{CC} and the V_{CV} generating from the mode control block are used in the currents reference block to control the three switches SW1, SW2 and SW3, respectively. Sending the I_{TC}, the I_{CC} and the I_{CV} to the charge control block in each charge mode (TC, CC, and CV).

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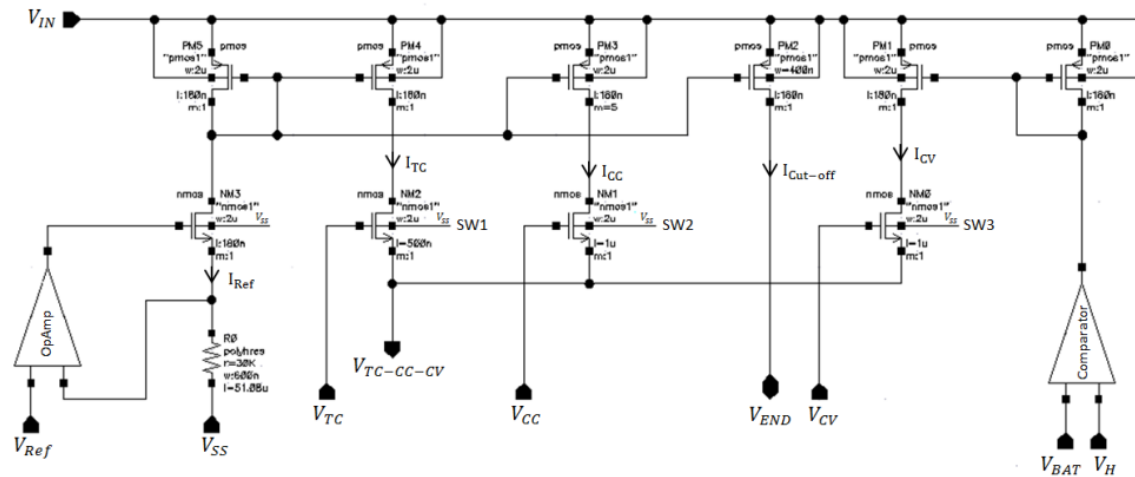
Figure 6. Schematic of the currents reference block under CADENCE software

2.3. Charge Control

The charge control circuit is illustrated in Figure 7. This block is utilized to generate a gate voltage (V_G) to the level-shifter with the gate-driver for driving the Power-PMOS in the each charge mode. The value of the V_G is varied with the current $I_{TC-CC-CV}$ by the current comparator which used in the design to compare between the current sensing I_{sense} (generating from the sensing current block) and the current $I_{TC-CC-CV}$ (generating from the currents reference block according to the each mode). The V_G is evaluated as the low voltage of the signal selector circuit. The $V_{control}$ (generating from the mode control block) is used for driving the selector circuit that consists of two transistors which is the PMOS (PM2) and the NMOS (NM0).

The last mode is the end of charge mode. This mode is made independently during a comparison between the cut-off current ($I_{cut-off}$) and the sensing current (I_{sense}). Therefore, if the $I_{cut-off}$ is lower than the I_{sense}, the end voltage (V_{END}) is at the low level that make the $V_{control}$ required level correspond to three charge modes (TC mode, CC mode and CV mode). Else if the $I_{cut-off}$ is higher than the I_{sense}, the V_{END} is at high level that make the $V_{control}$ in the low level which turns off the selector circuit. That means the V_G is at the highest level to make the charge process terminated.
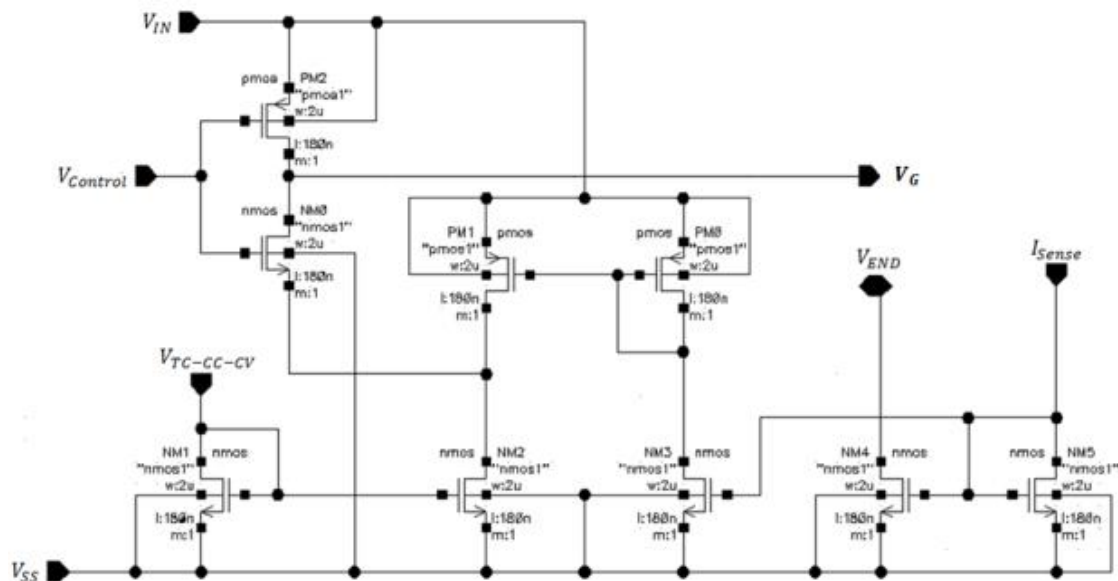

Figure 7. Schematic of the charge control block under CADENCE software

2.4. Level Shifter and Gate Driver

The level-shifter block is utilized to shift the low gate voltage (V_G) (generating from the charge control block) to a high voltage for driving the Power-PMOS. The level-shifter circuit is illustrated in Figure 8(a). Also, the gate-driver block is connected to the gate of the Power-PMOS which supplies power to the battery charge via the switching action, and then the suitable sum of current is regulated in the battery. The gate-driver circuit is illustrated in Figure 8(b). The level-shifter along side with the gate-driver achieves a rise time around 36 ps, a fall time around 36 ps and a propagation time around 0.25 ns [7].
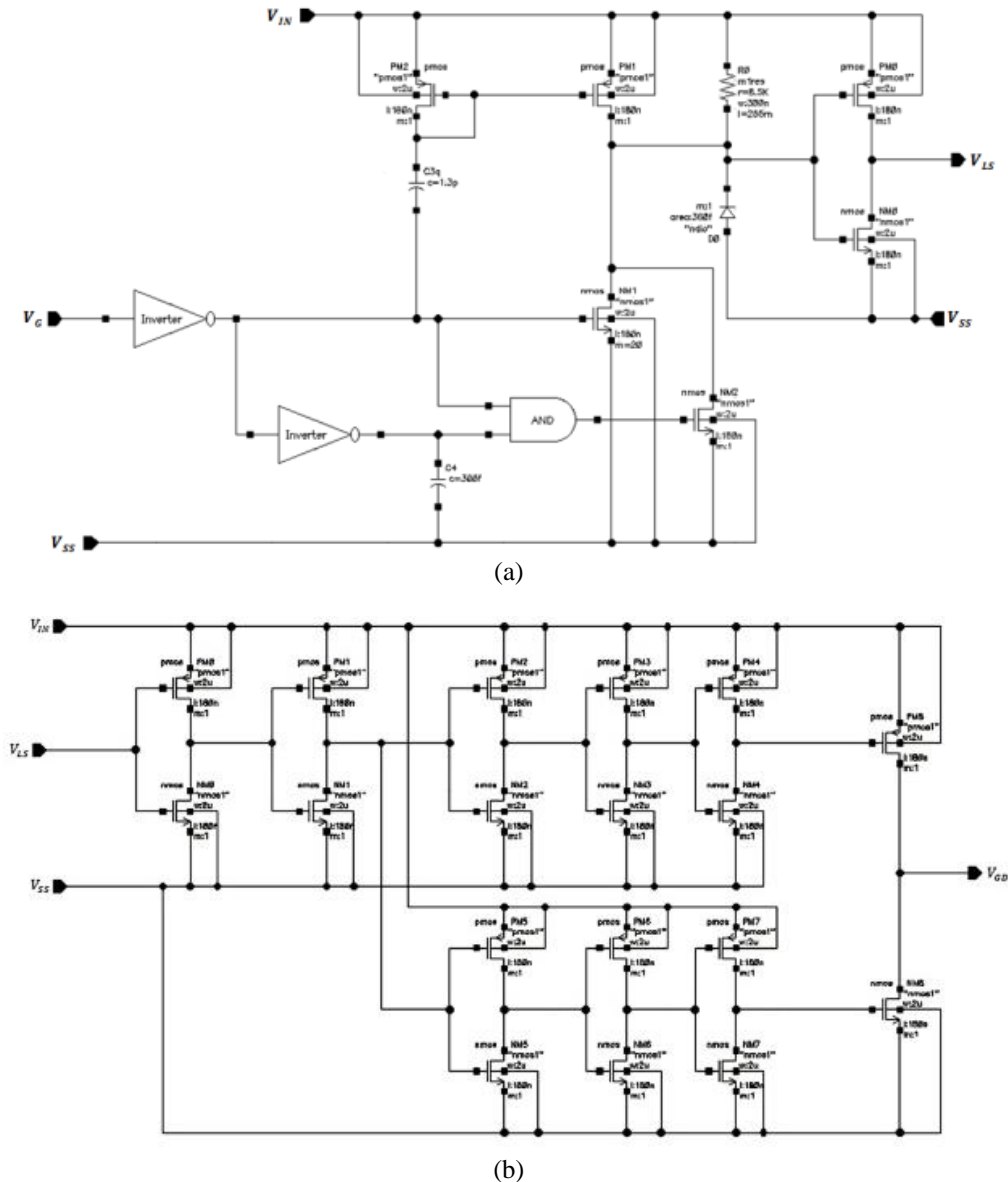

(a)

(b)

Figure 8. (a) Schematic of the level-shifter block under CADENCE software, (b) Schematic of the gate-driver block under CADENCE software

2.5. Current Sensing

Figure 9 shows the current sensing circuit, the PMOS transistor (PM0) used in the design like a charge current sensor. The OpAmp is utilized to remain drain voltage of the PMOS transistor (PM0) constant equal to the V_{BAT}. As a result, the I_{sense} has been always proportional to the current of the Power-PMOS.
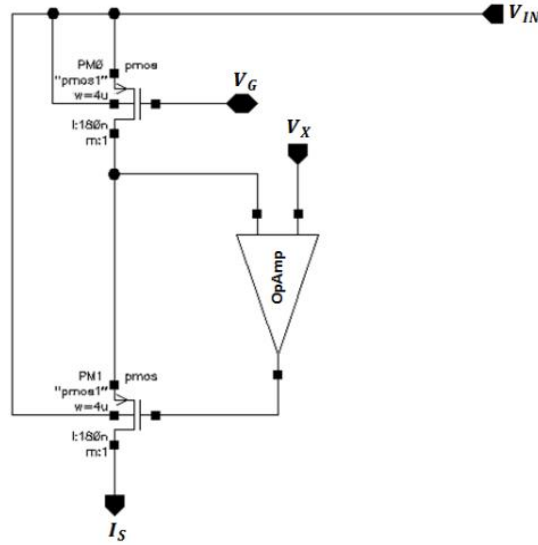
Figure 9. Schematic of the current-sensing block under CADENCE software

3. SIMULATION AND LAYOUT
3.1. Simulation

The proposed Li-Ion BCI design is realized by TSMC 180 nm CMOS technology under Cadence software. In this simulation, the battery capacity selected at 5000 mAh, the value of the V_L chosen equal 2.9 and the value of the V_H chosen equal 4.2. The waveforms of the mode control signals (The V_{TC}, the V_{CC} and the V_{CV}) in each charge mode are presented in Figure 10(a). It shows that V_{TC} is active in the TC mode, V_{CC} is active in the CC mode and V_{CV} is active in the CV mode. The simulation results of the I_{BAT} and the I_{sense} are presented in Figure 10(b).
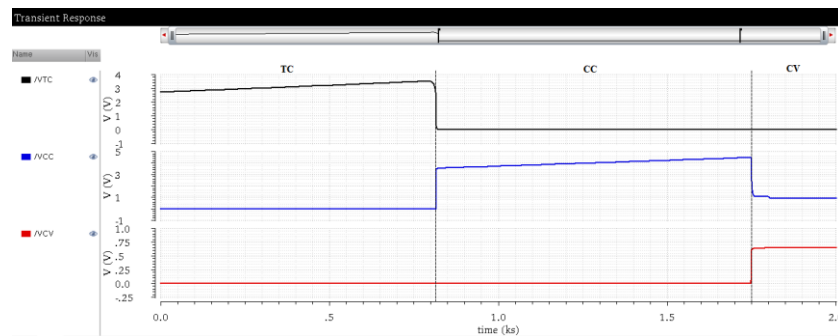
(a)
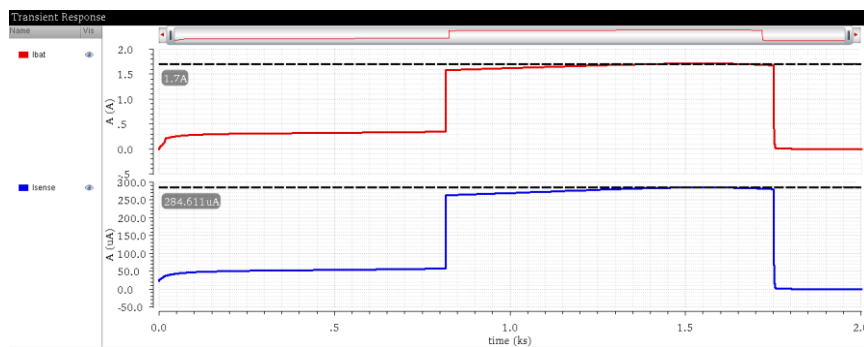
(b)

Figure 10. (a) Simulation results of the mode control, (b) Simulation results of the battery current (I_{BAT}) and the current sensing (I_{sense})

The simulation results of the V_{BAT} and the I_{BAT} in each charge mode (TC, CC and CV) of the proposed Li-Ion BCI are presented in Figure 11(a) and Figure 11(b), respectively. And also, we can observe from the simulation that the battery charges quickly within thirty-three minutes (2 kilo-second). The waveform of the V_{BAT} is presented in Figure 11(a), which shows that a variable value of the V_{BAT} is about 2.7 V to 4.2 V. Also, the waveform of the I_{BAT} is presented in Figure 11(b), which shows that the I_{BAT} in the TC mode is equal 342.7 mA and in the CC mode is equal 1.7 A. As well as the charging procedure is completed when the I_{BAT} is reaching the $I_{cut\text{-}off}$ value that equals about 20 mA.

Figure 12 illustrated the resulting curve of the power efficiency of the proposed Li-Ion BCI which achieving an efficiency equal 97% of the load current 1.7 A. It is calculated by equation:

$$\%\text{Efficiency} = \frac{P_{Out} \text{ (the output power in Watts)}}{P_{In} \text{ (the input power consumption in watts)}} \text{ X } 100 \tag{2}$$
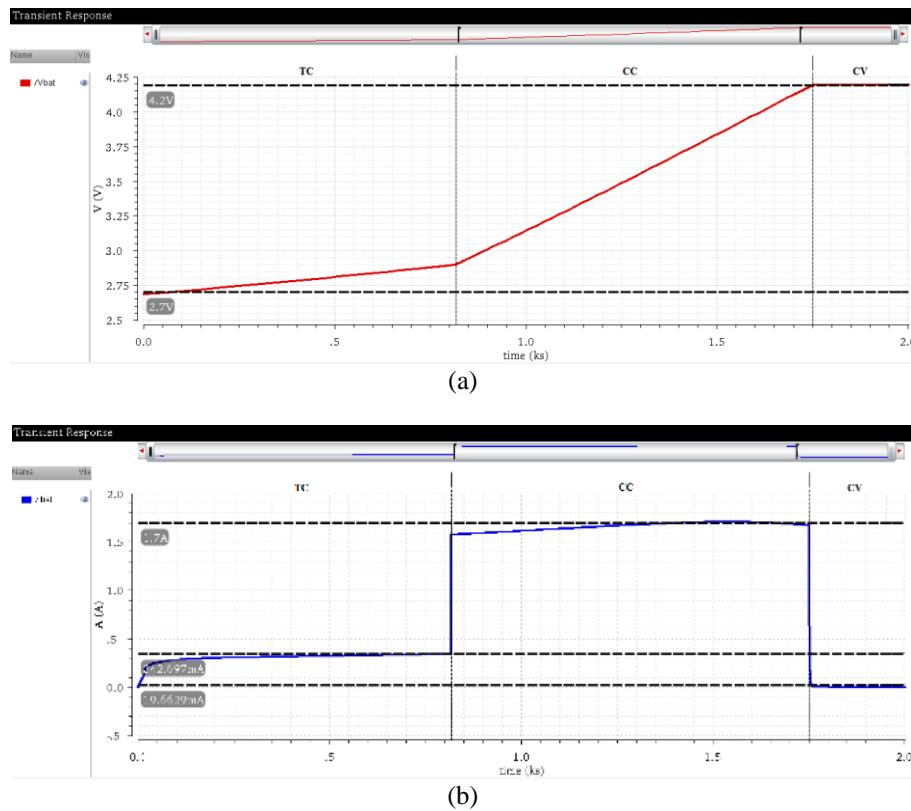

(a)

(b)

Figure 11. (a) The waveform of the battery voltage (V_{BAT}), (b) The waveform of the battery current (I_{BAT})
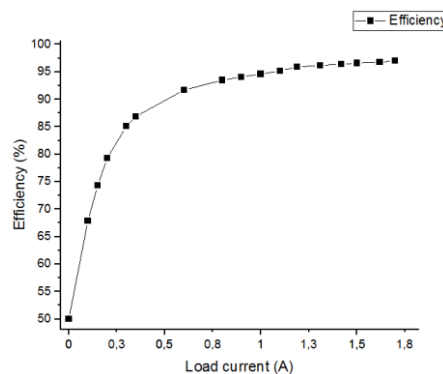
Figure 12. The resulting curve of the power efficiency

3.2. Layout

The layout of the proposed Li-Ion BCI is shown in Figure 13. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double layer guard rings. It is made by respecting the design rules (Density, DRM and MRC) and the designer constraint information (Cat match, text and constraint manager, etc.). It is occupying a total area of 0.03 mm^2.
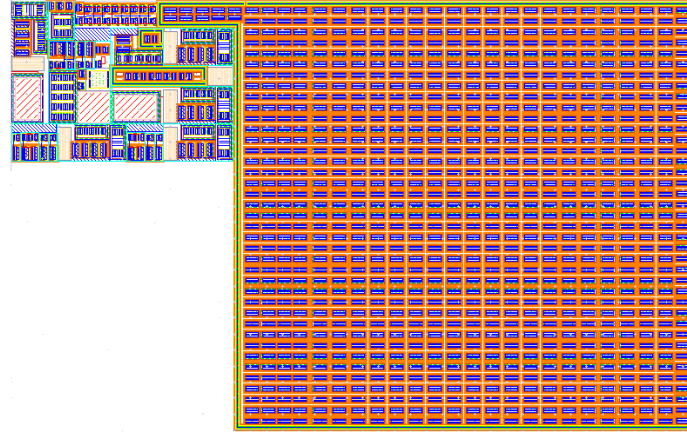

Figure 13. Layout of the proposed Li-Ion BCI

Table 1 is summarized of the simulation results found and a comparative analysis between the proposed Li-Ion battery charger interface and other works/references.

Table 1. Comparative analysis

Reference	[22] (2015)	[23] (2016)	[24] (2017)	[25] (2017)	[26] (2017)	[6] (2018)	[2] (2019)	This work
Topology	Adaptive LDO	Switching Based	LDO	Switching Based	Switching + LDO	Switching Based	Switching Based	Switching Based
Technology	180 nm CMOS	130 nm BICMOS	130 nm BICMOS	350 nm CMOS	180 nm CMOS	250 nm BCD	500 nm CMOS	TSMC 180 nm CMOS
Maximum Input Voltage, $V_{IN(max)}$ (V)	5	16	5	5.5	5.5	25	8.0-10.0	4.5
Output Range V_{BAT} (V)	2.5–4.2	2.5-4.2	3-4.3	2.3-4.2	2.8-4.2	6-22	2.5-4.2	2.7-4.2
Maximum Charging Current, $I_{BAT(max)}$ (A)	0.448	1.5	0.495	0.6	0.5	2.5	1.5	1.7
Peak Efficiency (%)	84	90	83.9	92.5	87.6	97	87.4 (CC) 88.6 (CV)	97
Die Size (mm^2)	1.62	12.25	1.41	2.7126	1.62	2.66	7.29	0.03

4. CONCLUSION

A low cost, low size and high speed charge of the proposed Li-Ion battery charger interface (BCI) have been successfully designed and implemented in TSMC 180 nm CMOS process. This study included the circuit design, simulation, analysis and layout design. The proposed Li-Ion BCI using switching-based technique achieves an output voltage V_{BAT} may range from 2.7 to 4.2 V according to an input voltage V_{IN} = 4.9 V, and also achieve a maximum charging battery current I_{BAT} equal 1.7 A. The time charging is only thirty three minutes, the peak efficiency reaches 97% and the total area is only 0.03 mm^2.

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